

JEDEC STANDARD

0.5V Low Voltage Swing Terminated Logic (LVSTL)

JESD8-35

November 2025

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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0.5V Low Voltage Swing Terminated Logic (LVSTL)

(From JEDEC Board Ballot JCB-25-64, formulated under the cognizance of the JC-16 committee on Interface Technology, item 159.03A).

1 Scope

This standard defines power supply voltage range, dc interface, switching parameter, and overshoot/undershoot for high speed low voltage swing terminated NMOS driver family digital circuits. The specifications in this standard represent a minimum set of interface specifications for low voltage terminated circuits.

The purpose of this standard is to provide a standard of specification for uniformity and multiplicity of sources.

2 Standard specifications

All voltages are referenced to ground except where noted.

3 LVSTL System Definition

LVSTL (Low Voltage Swing Terminated Logic) Driver and ODT System LVSTL I/O cell is comprised of pull-up, pull-down driver and a terminator. The basic cell is shown in **Figure 1**.

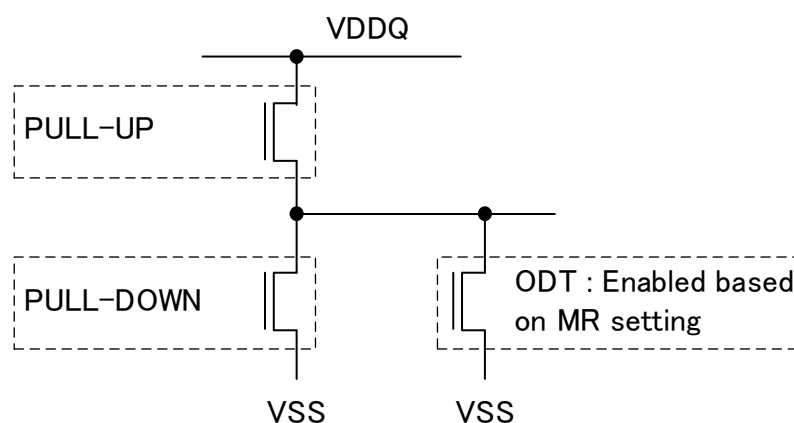


Figure 1 — LVSTL I/O Cell

4 Clause A: Hexagonal and Deterministic Mask

4.1 Recommended DC Operating Conditions

Table 1 — Recommended DC Operating Conditions

	Min	Typ	Max	Unit	Note
VDDxH	1.01	1.05	1.12	V	Internal circuit Power, DVFSH
VDDxL	0.97	0.90	0.97	V	Internal circuit Power, DVFSL
VDDQ Class 1,2	0.47	0.5	0.57	V	Driver Power range 1
VDDQ Class 3	0.27	0.3	0.37	V	Driver Power range 2

4.2 Driver Output Characteristics

Table 2 Pull-Up Characteristics

VOH _{PU} , nom	VOH, nom	Unit	Note
Class 1 VDDQ/2	250	mV	1
Class 2 VDDQ	500	mV	1
Class 3 VDDQ	300	mV	1
NOTE 1 VOH, nom values are based on a Typical VDDQ			

4.3 Input Level Characteristics for Class 1, Class 2, and Class 3

4.3.1 Hexagonal Rx Mask

Hexagonal Rx mask and single pulse definition are shown in the following.

4.3.1 Hexagonal Rx Mask (cont'd)

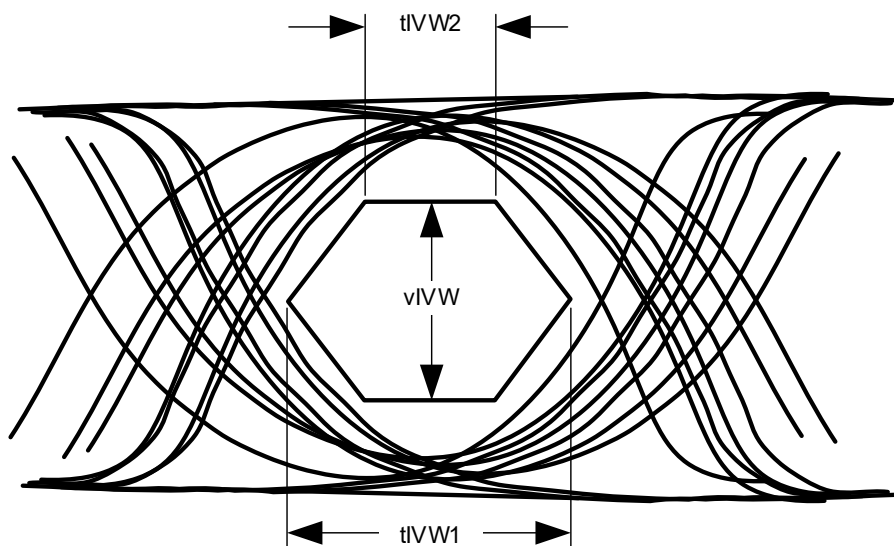


Figure 2 — Rx Mask Definition

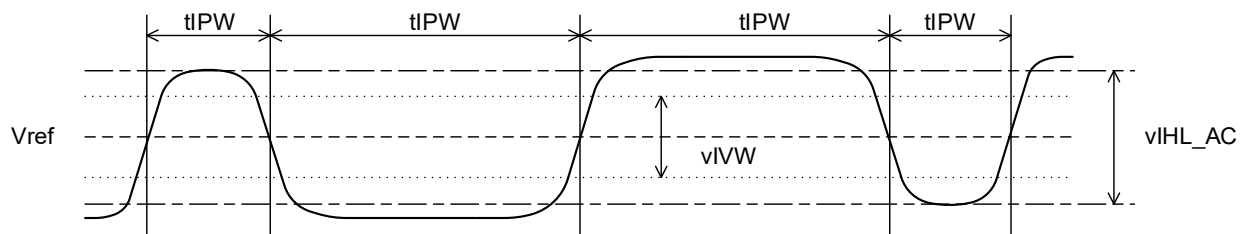
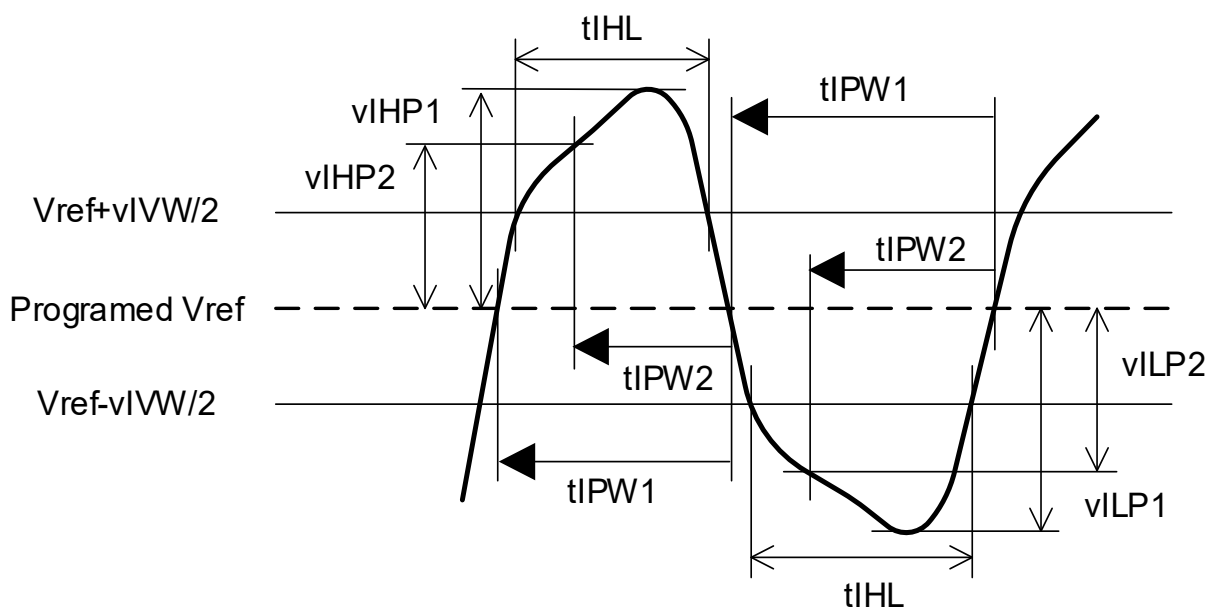


Figure 3 — Rx Single Pulse Definition for Range 1 to 4

4.3.1 Hexagonal Rx Mask (cont'd)



$$vIHL_AC/2 = vIHP1 = vILP1$$

$$\text{Programed Vref} = \% \text{ of Vref Mode Register code} * VDDQ$$

Figure 4 — Single Pulse Definition for Range 5

Table 3 — Single Pulse Definition for Range 5

Item	Symbol	Min/Max	Range 5	Unit	Note
Rx pulse width @ Vref	tIPW1	Min	Device depend	UI	1
Rx pulse reference	tIPW2	Min	Device depend	UI	1
Rx pulse width @ Vref +/- vIVW/2	tIHL	Min	Device depend	UI	1
Rx pulse amplitude from prog. Vref	vIHP1	Min	70	mV	
	vILP1	Max	-70	mV	
Rx early pulse amplitude from prog. Vref	vIHP2	Max	55	mV	
	vILP2	Min	-55	mV	
NOTE 1 Programmed Vref is defined as % of Vref Mode Register code * VDDQ					

4.3.1 Hexagonal Rx Mask (cont'd)

Table 4 —input Level Requirements

Item	Symbol	Min/Max	Range					Unit	Note
			1	2	3	4	5		
Rx Mask Height	vIVW	Min	155	140	120	100	80		
Rx Pulse amplitude	vIHL_AC	Min	190	140	140	140	N/A		

5 Clause B: Rectangle and Statistical Mask

5.1 Rectangle Mask Definition

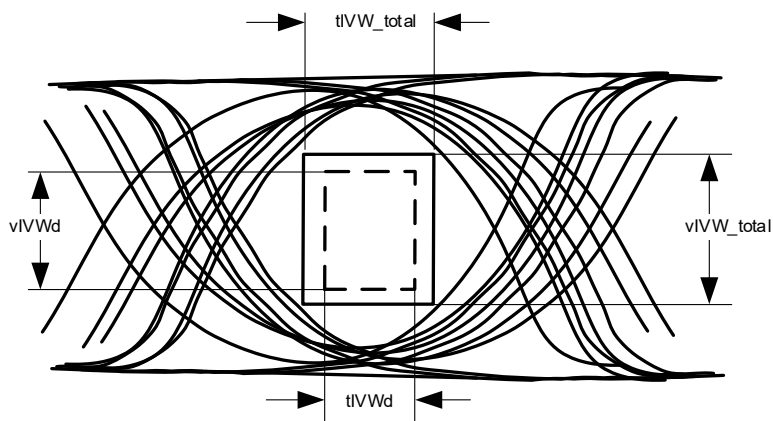


Figure 5 — Statistical Rectangle Mask Definition

5.1 Rectangle Mask Definition (cont'd)

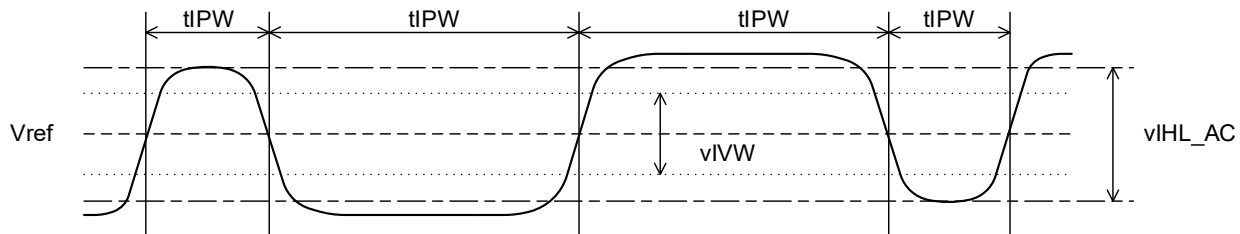
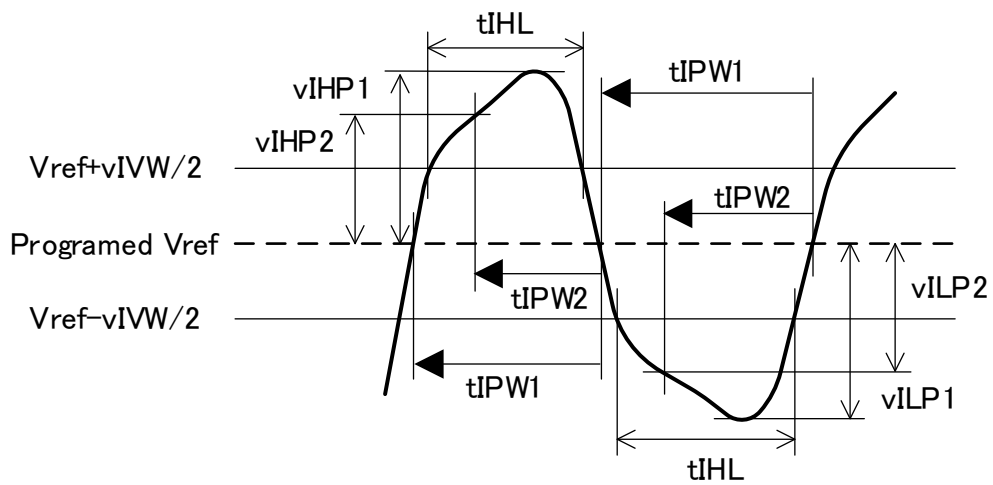


Figure 6 — Rx Single Pulse Definition



$$v_{IHL_AC}/2 = v_{IHP1} = v_{ILP1}$$

$$\text{Programed Vref} = \% \text{ of Mode Register code} * \text{VDDQ}$$

Figure 7 — Detailed Single Pulse Definition

5.1 Rectangle Mask Definition (cont'd)

Table 5 — Single Pulse Definition

Item	Symbol	Min/Max	Spec	Unit	Note
Rx pulse width @ Vref	tIPW1	Min	Device depend	UI	1
Rx pulse reference	tIPW2	Min	Device depend	UI	1
Rx pulse width @ Vref +/- vIVW/2	tIHL	Min	Device depend	UI	1
Rx pulse amplitude from prog. Vref	vIHP1	Min	70	mV	
	vILP1	Max	-70	mV	
Rx early pulse amplitude from prog. Vref	vIHP2	Max	55	mV	
	vILP2	Min	-55	mV	
NOTE 1 programmed Vref is defined as % of Vref Mode Register code * VDDQ					

Table 6 — Slew Rate Dependent Rx Mask Spec

Item	Symbol	Range 1D	Range 2D	Unit	Note
Rx mask height total	vIVW_total	135 (Slew Rate < 2V/ns)		mV	1,3
		135 (Slew Rate > =2Vns)	100 (Slew Rate > = 2 Vns)		
deterministic Rx mask height	vIVWd	TBD (Slew Rate < 2V/ns)		mV	
		TBD (Slew Rate > =2Vns)	TBD (Slew Rate > = 2 Vns)		
NOTE 1	vIVW_total and tIVW_total are defined by 1E-16 BER. tIVW_total and vIVW_total consider system PDN, clock jitter				
NOTE 2	tIVW_d and vIVW_d are defined at 1E-1 BER. tIVW_d and vIVW_d consider clock tree jitter and RX margin.				
NOTE 3	Slew rate measured at vIHP1 and vILP1.				

5.1 Rectangle Mask Definition (cont'd)

Table 7 — Slew Rate Independent Rx Mask Spec

[illegible]



Standard Improvement Form**JEDEC Standard JESD8-35**

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

-
2. Recommendations for correction:

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